IN THE CLAIMS

1. (Currently amended) A method of fabricating a flash memory device having a cell array region and a peripheral circuit region, the method comprising:

forming a device isolation layer at a predetermined region of a semiconductor substrate to define at least one first active region in the cell array region and a second active region in the peripheral circuit region;

forming a floating gate pattern covering the first active region and a gate conductive layer covering the peripheral circuit region;

forming a tunnel oxide layer having a first thickness, the tunnel oxide layer interposed between the floating gate pattern and the first active region;

forming a gate oxide layer having a second thickness, the gate oxide layer interposed between the gate conductive layer and the second active region, the second thickness different from the first thickness;

prior to formation of the tunnel oxide layer and the gate oxide layer, implanting impurity ions into the first and second active regions to adjust a threshold voltage of a MOS transistor;

prior to formation of the tunnel oxide layer and the gate oxide layer, implanting impurity ions into the first and second active regions to form a well;

sequentially forming an inter-gate dielectric layer and a control gate conductive layer on an entire surface of the substrate having the floating gate pattern and the gate conductive layer; and

selectively removing the control gate conductive layer and the inter-gate dielectric layer which are located in the peripheral circuit region, thereby exposing the gate conductive layer in the peripheral circuit region.

2. (Cancelled)

3. (Cancelled)

4. (Original) The method of claim 1, in which

the floating gate pattern and the gate conductive layer are formed of a doped polysilicon layer.

5. (Original) The method of claim 4, in which

the doped polysilicon layer is formed using an ion implantation technique.

6. (Original) The method of claim 5, in which

the ion implantation technique is performed using one of phosphor ions (P) and arsenic ions (As) as dopants.

7. (Original) The method of claim 4, in which

the doped polysilicon layer is formed using POCl3 as a dopant source.

8. (Original) The method of claim 1, in which

forming the device isolation layer, the floating gate pattern and the gate conductive layer includes:

forming a lower conductive layer on the entire surface of the semiconductor substrate;

sequentially patterning the lower conductive layer and the semiconductor to form a trench region at a predetermined region of the semiconductor substrate and concurrently define at least one first active region in the cell array region and a second active region in the peripheral circuit region;

forming a device isolation layer filling the trench region;

forming an upper conductive layer on the entire surface of the substrate having the device isolation layer; and

patterning the upper conductive layer to form a floating gate pattern covering the first active region and a gate conductive layer covering the peripheral circuit region, the floating gate pattern and the gate conductive layer being composed of a portion of the lower conductive layer and a portion of the upper conductive layer.

9. (Original) The method of claim 1, further comprising:

forming a metal silicide layer on the control gate conductive layer in the cell array region and the exposed gate conductive layer in the peripheral circuit region.

10. (Original) The method of claim 9, further comprising:

patterning the metal silicide layer, the control gate conductive layer, the inter-gate dielectric layer and the floating gate pattern that are located in the cell array region, thereby forming a word line crossing over the first active region and a floating gate interposed between the word line and the first active region; and

patterning the metal silicide layer and the gate conductive layer that are located in the peripheral circuit region, thereby forming a gate electrode crossing over the second active region.

11. (Previously presented) The method of claim 1, further comprising:

patterning the control gate conductive layer, the inter-gate dielectric layer and the floating gate pattern that are located in the cell array region, thereby forming a word line crossing over the first active region and a floating gate interposed between the word line and the first active region; and

patterning the gate conductive layer that is located in the peripheral circuit region, thereby forming a gate electrode crossing over the second active region.

12. (Currently amended) A method of fabricating a flash memory device having a cell array region and a peripheral circuit region, the method comprising:

forming a device isolation layer at a predetermined region of a semiconductor substrate to define at least one first active region in the cell array region and a second active region in the peripheral circuit region;

forming a floating gate pattern covering the first active region and a gate conductive layer covering the peripheral circuit region;

forming a tunnel oxide layer having a first thickness, the tunnel oxide layer interposed between the floating gate pattern and the first active region;

forming a gate oxide layer having a second thickness, the gate oxide layer interposed between the gate conductive layer and the second active region, the second thickness different from the first thickness;

prior to formation of the tunnel oxide layer and the gate layer, implanting impurity ions into the first and second active regions to adjust a threshold voltage of a MOS transistor;

prior to formation of the tunnel oxide layer and the gate oxide layer, implanting impurity ions into the first and second active regions to form a well;

sequentially forming an inter-gate dielectric layer and a control gate conductive layer on an entire surface of the substrate having the floating gate pattern and the gate conductive layer; and

stripping the control gate conductive layer and the inter-gate dielectric layer in the peripheral circuit region to expose the gate conductive layer in the peripheral circuit region.

13. (Previously presented) The method of claim 1, further comprising:

forming a metal silicide layer on the control gate conductive layer in the cell array region and the exposed gate conductive layer in the peripheral circuit region.

14. (Previously presented) The method of claim 1, wherein forming the tunnel oxide layer and forming the gate oxide layer comprises forming the gate oxide layer to a thickness different from that of the tunnel oxide layer